Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a ~~process or~~ processor in the data processing system, the method comprising:

responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction; [[and]]

responsive to a determination of metadata being present for the instruction, determining whether data is to be prefetched; and

responsive to a determination that data is to be prefetched, ~~selectively~~ prefetching data, from within a data structure using the metadata, into the cache in [[a]] the processor.

2. (Currently amended) The method of claim 1, wherein ~~the selectively prefetching step~~ determining whether data is to be prefetched comprises:

determining whether a number of outstanding cache misses [[are]] is less than a threshold; ~~present;~~ and wherein the prefetching step comprises:

prefetching the data [[if a]] when it is determined that the number of outstanding cache misses [[are]] is less than [[a]] the threshold.

3. (Currently amended) The method of claim 1, wherein ~~the selectively prefetching step~~ determining whether data is to be prefetched includes:

determining whether a number of cache lines chosen to be replaced is greater than a threshold; ~~to replace cache lines;~~ and wherein the prefetching step comprises:

prefetching the data [[if a]] when it is determined that the number of cache lines chosen to be replaced [[are]] is greater than [[a]] the threshold.

4. (Currently amended) The method of claim 1, wherein the ~~selectively~~ prefetching step includes: retrieving the data from within the data structure using a pointer and an offset value.

5. (Currently amended) The method of claim 1, wherein the ~~selectively~~ prefetching step includes: retrieving the data from the data structure using an address.

6. (Original) The method of claim 1, wherein the processor unit is selected from one of an instruction cache or a load/store unit.

7. (Original) The method of claim 1, wherein the cache is an instruction cache.

8. (Original) The method of claim 4, wherein the metadata includes the pointer and the offset value.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Currently amended) A data processing system for providing hardware assistance to prefetch data during execution of code by a ~~process or~~ processor in the data processing system, the data processing system comprising:

first determining means, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present for the instruction; [[and]]

~~selectively prefetching~~ second determining means, responsive to a determination of metadata being present for the instruction, for determining whether data is to be prefetched; and

prefetching means, responsive to a determination that data is to be prefetched, for ~~selectively~~ prefetching data, from within a data structure using the metadata, into the cache in [[a]] the processor.

13. (Currently amended) The data processing system of claim 12, wherein the ~~selectively prefetching~~ second determining means comprises:

first means for determining whether a number of outstanding cache misses [[are]] is less than a threshold; ~~present;~~ and wherein the prefetching means comprises:

second means for prefetching the data [[if a]] when it is determined that the number of outstanding cache misses [[are]] is less than [[a]] the threshold.

14. (Currently amended) The data processing system of claim 12, wherein the second determining ~~selectively prefetching~~ means includes:

first means for determining whether a number of cache lines chosen to be replaced is greater than a threshold; ~~to replace cache lines;~~ and wherein the prefetching means comprises:

second means for prefetching the data [[if a]] when it is determined that the number of cache lines chosen to be replaced [[are]] is greater than [[a]] the threshold.

15. (Currently amended) The data processing system of claim 12, wherein the ~~selectively~~ prefetching means includes:

retrieving means for retrieving the data from within the data structure using a pointer and an offset value.

16. (Currently amended) The data processing system of claim 12, wherein the ~~selectively~~ prefetching means includes:

retrieving means for retrieving the data from the data structure using an address.

17. (Original) The data processing system of claim 12, wherein the processor unit is selected from one of an instruction cache or a load/store unit.

18. (Currently amended) A computer program product in a recordable-type computer readable medium for providing hardware assistance to prefetch data during execution of code by a ~~process or~~ processor in the data processing system, the computer program product comprising:

first instructions, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present for the instruction; [[and]]

second instructions, responsive to a determination of metadata being present for the instruction, for determining whether data is to be prefetched; and

responsive to a determination that data is to be prefetched, ~~selectively~~ third instructions for prefetching data, from within a data structure using the metadata, into the cache in [[a]] the processor.

19. (Currently amended) The computer program product of claim 18, wherein the second instructions comprises:

first sub-instructions for determining whether a number of outstanding cache misses [[are]] is less than a threshold; ~~present;~~ and wherein the third instructions comprises:

second sub-instructions for prefetching the data [[if a]] when it is determined that the number of outstanding cache misses [[are]] is less than [[a]] the threshold.

20. (Currently amended) The computer program product of claim 18, wherein the second instructions includes:

first sub-instructions for determining whether a number of cache lines chosen to be replaced is greater than a threshold; ~~to replace cache lines;~~ and wherein the third instructions comprises:

second sub-instructions for prefetching the data ~~if a~~ when it is determined that the number of cache lines chosen to be replaced [[are]] is greater than [[a]] the threshold.

21. (Currently amended) The computer program product of claim 18, wherein the third ~~second~~ instructions includes:

sub-instructions for retrieving the data from within the data structure using a pointer and an offset value.

22. (Currently amended) The computer program product of claim 18, wherein the third ~~second~~ instructions includes:

sub-instructions for retrieving the data from the data structure using an address.

23. (Original) The computer program product of claim 18, wherein the processor unit is selected from one of an instruction cache or a load/store unit.